

ANNA UNIVERSITY TIRUCHIRAPPALLI

Tiruchirappalli – 620 024

Regulations 2007

Curriculum

M.E. APPLIED ELECTRONICS

SEMESTER I

S No.	Subject Code	Subject	L	T	P	Max. Marks
Theory						
1	MA5131	Applied Mathematics for Electronics Engineers	3	1	0	100
2	AN5101	Advanced Digital Signal Processing	3	1	0	100
3	AN5102	Advanced Digital System Design	3	1	0	100
4	AN5103	VLSI Design Techniques	3	0	0	100
5	AN5104	Advanced Microprocessors and Micro Controllers	3	0	0	100
6	E1***	Elective I	3	0	0	100
Practical						
7	AN5105	Electronics Design Laboratory I	0	0	4	100

SEMESTER II

S No.	Subject Code	Subject	L	T	P	Max. Marks
Theory						
1	AN5151	Analysis and Design of Analog Integrated Circuits	3	0	0	100
2	AN5152	Computer Architecture and Parallel Processing	3	0	0	100
3	AN5153	Digital Control Engineering	3	0	0	100
4	AN5154	Embedded Systems	3	0	0	100
5	E2***	Elective II	3	0	0	100
6	E3***	Elective III	3	0	0	100
Practical						
7	AN5155	Electronic Design Laboratory II	0	0	4	100

SEMESTER III

S No.	Subject Code	Subject	L	T	P	Max. Marks
Theory						
1	E4***	Elective IV	3	0	0	100
2	E5***	Elective V	3	0	0	100
3	E6***	Elective VI	3	0	0	100
Practical						
4	AN5251	Project Work Phase I	0	0	12	-

SEMESTER IV

S No.	Subject Code	Subject	L	T	P	Max. Marks
Theory						
1	AN5251	Project Work Phase II	0	0	24	600

LIST OF ELECTIVES

S No.	Subject Code	Subject	L	T	P	Max. Marks
1	AN5001	Digital Image Processing	3	0	0	100
2	AN5002	Neural Networks and Applications	3	0	0	100
3	AN5003	Robotics	3	0	0	100
4	VL5101	DSP Integrated Circuits	3	0	0	100
5	AN5005	ASIC Design	3	0	0	100
6	AN5006	Design and Analysis of Algorithms	3	0	0	100
7	AN5007	Reliability Engineering	3	0	0	100
8	AN5008	Internetworking Multimedia	3	0	0	100
9	AN5009	Electromagnetic Interference and Compatibility in System Design	3	0	0	100
10	AN5010	High Performance Communication Networks	3	0	0	100
11	CO5001	RF System Design	3	0	0	100
12	VL5002	Low Power VLSI Design	3	0	0	100
13	VL5003	VLSI Signal Processing	3	0	0	100
14	VL5005	Analog VLSI Design	3	0	0	100
15	VL5151	Computer Aided Design of VLSI Circuits	3	0	0	100

ANNA UNIVERSITY TIRUCHIRAPPALLI

Tiruchirappalli - 620 024

Regulations 2007

Syllabus

M.E. APPLIED ELECTRONICS AND ENGINEERING

SEMESTER I

MA5131 – APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

L	T	P
3	1	0

UNIT I LINEAR ALGEBRAIC EQUATIONS & EIGEN VALUE PROBLEMS 9

System of Equations – Solutions by Gauss Elimination Methods – Gauss Jordan and LU Decomposition Method Jacobi – Gauss Seidel Method – Eigen Values of Matrix by Jacobi and Power Method.

UNIT II THE WAVE EQUATIONS 9

Solution of Initial and Boundary Value Problems – Characteristics–D'Alembert's Solution– Significance of Characteristic Curves – Laplace Transform Solutions – for Displacement in a Long String – A long String under its Weight – Longitudinal Vibration of a Elastic Bar with Prescribed Force on one end – Free Vibrations of a String .

UNIT III SPECIAL FUNCTIONS 9

Bessel's Equation – Bessel Functions Legendre's Equation – Legendre Polynomials Rodrigue's Formula – Recurrence Relations – Generating Functions and Orthogonal Property for Bessel Functions – Legendre Polynomials.

UNIT IV RANDOM VARIABLES 9

One–Dimensional Random Variables – Moments and Moment Generating Function –Binomial Poisson– Uniform – Exponential Normal and Weibull Distribution – Two Dimensional Random Variables Marginal and Conditional Distribution Covariance – Correlation Coefficient – Function of One Dimensional and Two Dimensional Random Variables.

UNIT V QUEUING THEORY 9

Single and Multiple Server Markovian Queuing Models – Steady State System Size Probabilities– Little's Formula – Customer Impatience Priority Queues – M/G/1 Queuing System – PK Formula .

L: 45 T: 15 Total: 60

TEXT BOOKS

1. S. Narayanan T. K. Manichvachagam Pillay and G. Ramanaiah, “Advanced Mathematics for Engineering Students”, S.Viswanathan Pvt Ltd, Vol 2, 1986.
2. Taha H. A., “Operations Research An Introduction”, Sixth Edition, PHI, 1997.

REFERENCES

1. Sankara Rao K, “Introduction to Partial Differential Equation”, PHI, 1995.
2. Churchi R. V., “Operational Mathematics”, McGraw Hill, 1972.
3. Richard A. Johnson, “Miller and Freund's Probability and Statistics for Engineers”, Fifth Edition, PHI, 1994.

AN5101 – ADVANCED DIGITAL SIGNAL PROCESSING

L T P
3 1 0

[Review of discrete time signals and systems - DFT and FFT - Z-Transform - Digital Filters is recommended]

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes - Ensemble averages - Stationary processes - Autocorrelation and Auto covariance matrices - Parseval's Theorem - Wiener -Khintchine Relation - Power Spectral Density - Periodogram Spectral Factorization - Filtering random processes - Low Pass Filtering of White Noise - Parameter estimation - Bias and consistency.

UNIT II SPECTRUM ESTIMATION 9

Estimation of spectra from finite duration signals - Non-Parametric Methods -Correlation Method - Periodogram Estimator - Performance Analysis of Estimators -Unbiased - Consistent Estimators - Modified periodogram - Bartlett and Welch methods - Blackman - Tukey method - Parametric Methods - AR - MA - ARMA model based spectral estimation - Parameter Estimation - Yule-Walker equations - Solutions using Durbin's algorithm

UNIT III LINEAR ESTIMATION AND PREDICTION 9

Linear prediction - Forward and backward predictions - Solutions of the Normal equations - Levinson - Durbin algorithms - Least mean squared error criterion -Wiener filter for filtering and prediction - FIR Wiener filter and Wiener IIR filters - Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 9

FIR adaptive filters - Adaptive filter based on steepest descent method - Widrow -Hoff LMS adaptive algorithm - Normalized LMS - Adaptive channel equalization - Adaptive echo cancellation - Adaptive noise cancellation - Adaptive recursive filters (IIR) - RLS adaptive filters - Exponentially weighted RLS - Sliding window RLS.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of change of sampling rate - Interpolation and Decimation - Decimation by an integer factor - Interpolation by an integer factor - Sampling rate conversion by a rational factor - Filter implementation for sampling rate conversion - Direct form FIR structures - Polyphase filter structures - Time-variant structures - Multistage implementation of multirate system - Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

L: 45 T: 15 Total: 60

TEXT BOOKS

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc., Singapore, 2002.
2. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 2002.

REFERENCES

1. John G. Proakis et.al. "Algorithms for Statistical Signal Processing", Pearson Education, 2002.
2. Dimitris G. Manolakis et.al. "Statistical and adaptive signal Processing", McGraw Hill, Newyork, 2000.
3. Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson Education, Inc.,Second Edition, 2004.(For Wavelet Transform Topic)

AN5102 – ADVANCED DIGITAL SYSTEM DESIGN

L T P
3 1 0

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN - State Stable Assignment and Reduction - Design of CSSN - Design of Iterative Circuits - ASM Chart - ASM Realization.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction - Races in ASC - State Assignment - Problem and the Transition Table - Design of ASC - Static and Dynamic Hazards - Essential Hazards - Data Synchronizers - Designing Vending Machine Controller - Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method - Path Sensitization Method - Boolean Difference Method - Kohavi Algorithm - Tolerance Techniques - The Compact Algorithm - Practical PLA's - Fault in PLA - Test Generation - Masking Cycle - DFT Schemes - Built-in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

EPLD to Realize a Sequential Circuit - Programmable Logic Devices - Designing a Synchronous Sequential Circuit using a GAL - EPLD - Realization State machine using PLD - FPGA - Xilinx FPGA - Xilinx 2000 - Xilinx 3000

UNIT V SYSTEM DESIGN USING VHDL 9

VHDL Description of Combinational Circuits - Arrays - VHDL Operators - Compilation and Simulation of VHDL Code - Modeling using VHDL - Flip Flops - Registers - Counters - Sequential Machine - Combinational Logic Circuits - VHDL Code for - Serial Adder- Binary Multiplier - Binary Divider - Complete Sequential Systems - Design of a Simple Microprocessor.

L: 45 T: 15 Total: 60

TEXT BOOKS

1. John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2001.
2. Mark Zwolinski, "Digital System Design with VHDL", Pearson Education, 2004.

REFERENCES

1. Donald G. Givone, "Digital principles and Design", Tata McGraw Hill, 2002.
2. Charles H. Roth Jr., "Digital System Design using VHDL" Thomson Learning, 1998.
3. Stephen Brown and Zvonk Vranesic, "Fundamentals of Digital Logic with VHDL Design", Tata McGraw Hill, 2002.
4. Navabi .Z, "VHDL Analysis and Modeling of Digital Systems", McGraw International, 1998.

AN5104 – ADVANCED MICROPROCESSORS AND MICRO CONTROLLERS

L T P
3 0 0

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction set - Data formats - Instruction formats - Addressing modes - Memory hierarchy - register file - Cache - Virtual memory and paging - Segmentation - Pipelining - The instruction pipeline - Pipeline hazards - Instruction level parallelism - Reduced instruction set - Computer principles - RISC versus CISC - RISC properties - RISC evaluation - On-chip register files versus cache evaluation .

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE - PENTIUM 9

The software model - Functional description - CPU pin descriptions - RISC concepts - Bus operations - Super scalar architecture - Pipe lining - Branch prediction - The instruction and caches - Floating point unit - protected mode operation - Segmentation - paging - Protection - Multitasking - Exception and interrupts - Input /Output - Virtual 8086 model - Interrupt processing - Instruction types - Addressing modes - Processor flags - Instruction set - Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

The ARM architecture - ARM assembly language program - ARM organization and implementation - The ARM instruction set - The thumb instruction set - ARM CPU cores.

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS 9

Instructions and addressing modes - operating modes - Hardware reset - Interrupt system - Parallel I/O ports - Flags - Real time clock - Programmable timer - Pulse accumulator - Serial communication interface - A/D converter - Hardware expansion - Assembly language Programming

UNIT V PIC MICRO CONTROLLER 9

CPU architecture - Instruction set - Interrupts - Timers - I/O port expansion - I²C bus for peripheral chip access - A/D converter - UART

Total: 45

TEXT BOOKS

1. Gene H. Miller, “Micro Computer Engineering”, Pearson Education, 2003.
2. John B. Peatman, “Design with PIC Microcontroller”, Prentice Hall, 1997.

REFERENCES

1. Daniel Tabak , “Advanced Microprocessors”, McGraw Hill.Inc., 1995
2. James L. Antonakos, “The Pentium Microprocessor”, Pearson Education, 1997.
3. Steve Furber, “ARM System on Chip architecture”, Addison Wesley, 2000.
4. Barry B. Breg, “The Intel Microprocessors Architecture, Programming and Interfacing”,PHI, 2002.

AN5105 – ELECTRONICS DESIGN LABORATORY I

L	T	P
0	0	4

1. System design using PIC Microcontroller.
2. Implementation of Adaptive Filters- periodogram and multistage multirate system in DSP Processor
3. Simulation of QMF using Simulation Packages
4. Modeling of Sequential Digital system using VHDL.
5. Modeling of Sequential Digital system using Verilog.
6. Design and Implementation of ALU using FPGA.
7. Simulation of NMOS and CMOS circuits using SPICE.
8. System design using 16- bit Microprocessor.

SEMESTER II

AN5151 – ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

L	T	P
3	0	0

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction - Large signal behavior of bipolar transistors - Small signal model of bipolar transistor - Large signal behavior of MOSFET - Small signal model of the MOS transistors - Short channel effects in MOS transistors - Weak inversion in MOS transistors - Substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources - Analysis of difference amplifiers with active load using BJT and FET - Supply and temperature independent biasing techniques - Voltage references - Output stages - Emitter follower - Source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 9

Analysis of operational amplifiers circuit - Slew rate model and high frequency analysis - Frequency response of integrated circuits - Single stage and multistage amplifiers - Operational amplifier noise.

UNIT IV ANALOG MULTIPLIER AND PLL 9

Analysis of four quadrant and variable trans conductance multiplier - Voltage controlled oscillator - Closed loop analysis of PLL - Monolithic PLL design in integrated circuits - Sources of noise - Noise models of Integrated - Circuit Components - Circuit Noise Calculations - Equivalent Input Noise Generators - Noise Bandwidth - Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

MOS Current Mirrors - Simple- Cascode - Wilson and Widlar current source - CMOS Class AB output stages - Two stage MOS Operational Amplifiers - with Cascode - MOS Telescopic - Cascode Operational Amplifier - MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

Total: 45

TEXT BOOKS

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", 4th Edition, Willey International, 2002.
2. Nandita Dasgupta, Amitava Dasgupta, "Semiconductor Devices - Modelling and Technology", Prentice Hall of India pvt. Ltd, 2004.

REFERENCES

1. Behzad Razavi, "Principles of data conversion system design", S.Chand and Company Ltd, 2000
2. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & Sons Inc, 2003.
3. Phillip E. Allen Douglas R. Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, 2003.

AN5152 – COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

L	T	P
3	0	0

UNIT I PRINCIPLES OF PARALLEL PROCESSING 9

Multiprocessors and Multicomputers - Multivector and SIMD Computers - PRAM and VLSI Models - Conditions of Parallelism - Program Partitioning and scheduling-program flow mechanisms - Parallel processing applications - Speed up performance law.

UNIT II PROCESSOR AND MEMORY ORGANIZATION 9

Advanced processor technology - Superscalar and vector processors - Memory hierarchy technology - Virtual memory technology - Cache memory organization - Shared memory organization.

UNIT III PIPELINE AND PARALLEL ARCHITECTURE 9

Linear pipeline processors - Non linear pipeline processors - Instruction pipeline design - Arithmetic design - Superscalar and super pipeline design - Multiprocessor system interconnects - Message passing mechanisms.

UNIT IV VECTOR- MULTITHREAD AND DATAFLOW ARCHITECTURE 9

Vector processing principle – Multivector Multiprocessors - Compound Vector processing - Principles of multithreading - Fine grain multicomputers - Scalable and multithread architectures - Dataflow and hybrid architectures.

UNIT V SOFTWARE AND PARALLEL PROCESSING 9

Parallel programming models - Parallel languages and compilers - Parallel programming environments - Synchronization and multiprocessing modes - Message passing program development - Mapping programs onto multicomputers - Multiprocessor UNIX design goals - MACH/OS kernel architecture - OSF/1 architecture and applications.

Total: 45

TEXT BOOK

1. Kai Hwang, “Advanced Computer Architecture”, TMH, 2001.

REFERENCES

1. William Stallings, “Computer Organization and Architecture”, McMillan Publishing Company, 1990.
2. M.J. Quinn, “Designing efficient Algorithms for parallel computer”, McGraw Hill International, 1994.

AN5153 – DIGITAL CONTROL ENGINEERING

L T P
3 0 0

UNIT I FUNDAMENTALS

9

Review of frequency and time response analysis and specifications of control systems - Need for controllers - Continuous time compensations - Continuous time PI – PD - PID controllers - Digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL

9

Sampling - Time and frequency domain description – Aliasing - Hold operation - Mathematical model of sample and hold - Zero and first order hold - Factors limiting the choice of sampling rate - Reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM

9

Difference equation description - Z-transform method of description - Pulse transfer function - Time and frequency response of discrete time control systems - Stability of digital control systems - Jury's stability test - State variable concepts - First companion - Second companion - Jordan canonical models - Discrete state variable models - Elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS

9

Review of principle of compensator design - Z-plane specifications - Digital compensator design using frequency response plots - Discrete integrator - Discrete differentiator - Development of digital PID controller - Transfer function- Design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS

9

Algorithm development of PID control algorithms - Software implementation - Implementation using microprocessors and microcontrollers - Finite word length effects - Choice of data acquisition systems - Microcontroller based temperature control systems - Microcontroller based motor speed control systems.

Total: 45

TEXT BOOKS

1. M. Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, "Constantive Houpios Linear Control System Analysis and Design", Tata Mc Graw Hill, 1995.

REFERENCES

1. Kenneth J. Ayala, "The 8051 Microcontroller, Architecture, Programming and Applications", 2nd Edition, Penram International, 1996.

AN5154 – EMBEDDED SYSTEM

L T P
3 0 0

UNIT I EMBEDDED ARCHITECTURE

9

Embedded Computers - Characteristics of Embedded Computing Applications - Challenges in Embedded Computing system design - Embedded system design process – Requirements – Specification - Architectural Design - Designing Hardware and Software Components - System Integration - Formalism for System Design - Structural Description - Behavioral Description - Design Example - Model Train Controller.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM

9

ARM processor - processor and memory organization - Data operations - Flow of Control - SHARC processor - Memory organization - Data operations - Flow of Control - parallelism with instructions - CPU Bus configuration - ARM Bus - SHARC Bus- Memory devices - Input/output devices - Component interfacing - designing with microprocessor development and debugging - Design Example - Alarm Clock.

UNIT III NETWORKS

9

Distributed Embedded Architecture - Hardware and Software Architectures - Networks for embedded systems - I²C - CAN Bus - SHARC link ports - Ethernet - Myrinet – Internet - Network-Based design - Communication Analysis - system performance Analysis - Hardware platform design - Allocation and scheduling - Design Example - Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS

9

Clock driven Approach - Weighted Round Robin Approach - Priority driven Approach - Dynamic Versus Static systems - Effective release times and deadlines - Optimality of the Earliest deadline first (EDF) algorithm - Challenges in validating timing constraints in priority driven systems - Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES

9

Design Methodologies - Requirement Analysis – Specification - System Analysis and Architecture Design - Quality Assurance - Design Example - Telephone PBX - System Architecture - Ink jet printer - Hardware Design and Software Design - Personal Digital Assistants - Set-top Boxes.

Total: 45

TEXT BOOK

1. Wayne Wolf, “Computers as Components- Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2001.

REFERENCES

1. Jane W. S. Liu, “ Real-Time systems” , Pearson Education Asia, 2000.
2. C. M. Krishna and K. G. Shin , “Real-Time Systems” , McGraw Hill, 1997.
3. Frank Vahid and Tony Givargi, “Embedded System Design A Unified Hardware/Software Introduction”, John Wiley & Sons, 2000.

AN5155 – ELECTRONIC DESIGN LABORATORY II

L	T	P
0	0	3

1. System design using PLL.
2. System design using CPLD.
3. Alarm clock using embedded micro controller.
4. Model train controller using embedded micro controller.
5. Elevator controller using embedded micro controller.
6. Simulation of Non adaptive Digital Control System using MAT LAB control system toolbox.
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox.

ELECTIVES

AN5001 – DIGITAL IMAGE PROCESSING

L	T	P
3	0	0

UNIT I DIGITAL IMAGE FUNDAMENTALS

9

Elements of digital image processing systems - Elements of visual perception - Psycho visual model - Brightness - Contrast - Hue - Saturation - Mach band effect - Color image fundamentals - RGB-HSI models - Image sampling - Quantization - Dither - Two-dimensional mathematical preliminaries.

UNIT II IMAGE TRANSFORMS

9

1D DFT - 2D transforms - DFT - DCT - Discrete Sine - Walsh - Hadamard - Slant - Haar - KLT - SVD - Wavelet Transform.

UNIT III ENHANCEMENT AND RESTORATION

9

Histogram modification and specification techniques - Noise distributions - Spatial averaging - Directional Smoothing – Median - Geometric mean - Harmonic mean - Contraharmonic and Yp mean filters - Homomorphic filtering - Color image enhancement - Image Restoration - Degradation model - Unconstrained and Constrained restoration - Inverse filtering - Removal of blur caused by uniform linear motion - Wiener filtering - Geometric transformations - Spatial transformations - Gray Level interpolation.

UNIT IV IMAGE SEGMENTATION AND RECOGNITION

9

Edge detection - Image segmentation by region growing - Region splitting and merging - Edge linking - Image Recognition - Patterns and pattern classes - Matching by minimum distance classifier - Matching by correlation - Back Propagation Neural Network - Neural Network applications in Image Processing.

UNIT V IMAGE COMPRESSION

9

Need for data compression - Huffman - Run Length Encoding - Shift codes - Arithmetic coding - Vector Quantization - Block Truncation Coding - Transform Coding - DCT and Wavelet - JPEG - MPEG – Standards - Concepts of Context based Compression.

Total: 45

TEXT BOOKS

1. Rafael C. Gonzalez, Richard E. Woods, ‘Digital Image Processing’, Second Edition, Pearson Education Inc., 2004.
2. Anil K. Jain, ‘Fundamentals of Digital Image Processing’, Prentice Hall of India, 2002.

REFERENCES

1. David Salomon , “Data Compression The Complete Reference”, 2nd Edition, Springer Verlag , New York Inc., 2001.
2. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins, “Digital Image Processing using MATLAB”, Pearson Education, Inc., 2004.
3. William K. Pratt, “Digital Image Processing”, John Wiley, NewYork, 2002.
4. Milman Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing Analysis and Machine Vision”, 2nd edition, Brooks/Cole, Vikas Publishing House, 1999.

UNIT I BASIC LEARNING ALGORITHMS 9

Biological Neuron - Artificial Neural Model - Types of activation functions - Architecture - Feedforward and Feedback - Learning Process - Error Correction Learning - Memory Based Learning - Hebbian Learning - Competitive Learning - Boltzman Learning - Supervised and Unsupervised Learning - Learning Tasks - Pattern Space - Weight Space - Pattern Association - Pattern Recognition - Function Approximation - Control - Filtering - Beamforming - Memory - Adaptation - Statistical Learning Theory - Single Layer Perceptron - Perceptron Learning Algorithm - Perceptron Convergence Theorem - Least Mean Square Learning Algorithm - Multilayer Perceptron - Back Propagation Algorithm - XOR problem - Limitations of Back Propagation Algorithm.

UNIT II RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES 9

RADIAL BASIS FUNCTION NETWORKS

Cover's Theorem on the Separability of Patterns - Exact Interpolator - Regularization Theory - Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications - XOR Problem - Image Classification.

SUPPORT VECTOR MACHINES

Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns - Support Vector Machine for Pattern Recognition - XOR Problem - \square -insensitive Loss Function - Support Vector Machines for Nonlinear Regression.

UNIT III COMMITTEE MACHINES 9

Ensemble Averaging - Boosting - Associative Gaussian Mixture Model - Hierarchical Mixture of Experts Model(HME) - Model Selection using a Standard Decision Tree - A Priori and Postpriori Probabilities - Maximum Likelihood Estimation - Learning Strategies for the HME Model - EM Algorithm - Applications of EM Algorithm to HME Model.

NEURODYNAMICS SYSTEMS

Dynamical Systems - Attractors and Stability - Non-linear Dynamical Systems - Lyapunov Stability - Neurodynamical Systems - The Cohen-Grossberg Theorem.

UNIT IV ATTRACTOR NEURAL NETWORKS 9

Associative Learning - Attractor Neural Network Associative Memory - Linear Associative Memory - Hopfield Network - Content Addressable Memory - Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks - Simulated Annealing - Boltzmann Machine - Bidirectional Associative Memory - BAM Stability Analysis - Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS - Continuous BAMs - Adaptive BAMs - Applications.

ADAPTIVE RESONANCE THEORY

Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma - Recurrent On-center-Off surround Networks - Building Blocks of Adaptive Resonance - Substrate of Resonance Structural Details of Resonance Model - Adaptive Resonance Theory – Applications.

UNIT V SELF ORGANISING MAPS

9

Self-organizing Map - Maximal Eigenvector Filtering - Sanger's Rule - Generalized Learning Law - Competitive Learning - Vector Quantization - Mexican Hat Networks - Self-organizing Feature Maps – Applications.

PULSED NEURON MODELS

Spiking Neuron Model - Integrate-and-Fire Neurons - Conductance Based Models - Computing with Spiking Neurons.

Total: 45

TEXT BOOKS

1. Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw Hill Publishing Company Limited, 2004.
2. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2nd edition, Addison Wesley Longman (Singapore) Private Limited, 2001.

REFERENCES

1. Martin T. Hagan, Howard B. Demuth, and Mark Beale, "Neural Network Design", Thomson Learning, 2003.
2. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications and Programming Techniques", Pearson Education (Singapore) Private Limited, 2003.

VL5101 – DSP INTEGRATED CIRCUIT

L T P
3 0 0

UNIT I DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors - Application specific IC's for DSP - DSP systems - DSP system design - Integrated circuit design - MOS transistors - MOS logic - VLSI process technologies - Trends in CMOS technologies.

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing - Sampling of analog signals - Selection of sample frequency - Signal processing systems - Frequency response - Transfer functions - Signal flow graphs - Filter structures - Adaptive DSP algorithms - DFT - The Discrete Fourier Transform – FFT - The Fast Fourier Transform Algorithm - Image coding - Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters - FIR filter structures - FIR chips - IIR filters - Specifications of IIR filters - Mapping of analog transfer functions - Mapping of analog filter structures - Multirate systems - Interpolation with an integer factor L - Sampling rate change with a ratio L/M - Multirate filters - Finite word length effects - Parasitic oscillations - Scaling of signal levels - Round-off noise - Measuring round-off noise - Coefficient sensitivity- Sensitivity and noise.

UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multicomputers - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit - serial PEs.

UNIT V NUMBER SYSTEMS - ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system - Redundant Number system - Residue Number System - Bit-parallel and Bit-Serial arithmetic - Basic shift accumulator - Reducing the memory size - Complex multipliers - Improved shift-accumulator - Layout of VLSI circuits - FFT processor - DCT processor and Interpolator as case studies

Total: 45

TEXT BOOKS

1. A.V. Oppenheim et.al, “Discrete-time Signal Processing”, Pearson education, 2000.
2. Keshab K.Parhi, “VLSI digital Signal Processing Systems design and Implementation”, John Wiley & Sons, 1999.

REFERENCES

1. Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York, 1999.
2. Emmanuel C. Ifeachor, Barrie W. Jervis, “Digital signal processing, A practical approach”, 2nd edition, Prentice Hall, 2001.

AN5005 – ASIC DESIGN

L T P
3 0 0

UNIT I FUNDAMENTALS TO ASICS- CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance - Logical effort -Library cell design - Library architecture .

UNIT II PROGRAMMABLE ASICS - PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT - PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT - Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX - Design systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language - PLA tools – EDIF - CFI design representation.

UNIT IV LOGIC SYNTHESIS- SIMULATION AND TESTING 9

Verilog and logic synthesis - VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION- FLOOR PLANNING- PLACEMENT AND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.

Total: 45

TEXT BOOKS

1. Wayne Wolf, “FPGA,Based System Design”, Prentice Hall PTR, 2004.
2. R. Rajsuman, “System-on-a-Chip Design and Test”, Santa Clara, CA, Artech House Publishers, 2000.

REFERENCES

1. M.J.S. Smith, "Application Specific Integrated Circuits", Addison Wesley Longman Inc, 1997.
2. Farzad Nekoogar and Faranak Nekoogar, “From ASICs to SOCs, A Practical Approach”, Prentice Hall PTR, 2003.
3. F. Nekoogar, “Timing Verification of Application-Specific Integrated Circuits (ASICs)”, Prentice Hall PTR, 1999.

AN5006 – DESIGN AND ANALYSIS OF ALGORITHMS

L	T	P
3	0	0

UNIT I FUNDAMENTALS

9

Polynomial and Exponential algorithms - big "oh" and small "oh" notation - exact algorithms and heuristics - direct / indirect / deterministic algorithms - static and dynamic complexity - stepwise refinement.

UNIT II DESIGN TECHNIQUES

9

Subgoals method - working backwards - work tracking - branch and bound algorithms for traveling salesman problem and knapsack problem - hill climbing techniques - divide and conquer method - dynamic programming - greedy methods.

UNIT III SEARCHING AND SORTING

9

Sequential search - binary search - block search - Fibonacci search - bubble sort - bucket sorting - quick sort - heap sort - average case and worst case behavior - FFT.

UNIT IV GRAPH ALGORITHMS

9

Minimum spanning tree - shortest path algorithms - R-connected graphs - Even's and Kleitman's algorithms - ax-flow min cut theorem - Steiglitz's link deficit algorithm.

UNIT V SELECTED TOPICS

9

NP Completeness Approximation Algorithms - NP Hard Problems - Strassen's Matrix Multiplication Algorithms - Magic Squares - Introduction To Parallel Algorithms and Genetic Algorithms - Monte-Carlo Methods - Amortised Analysis.

Total: 45

TEXT BOOKS

1. Sara Baase, "Computer Algorithms - Introduction to Design and Analysis", Addison Wesley, 1988.
2. T.H. Corman, C.E. Leiserson and R.L. Rioest, "Introduction to Algorithms", Mc Graw Hill, 1994.

REFERENCES

1. E. Horowitz and S .Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
2. D.E. Goldberg, "Genetic Algorithms - Search Optimization and MachineLearning", Addison Wesley, 1989.

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9

Statistical distribution - statistical confidence and hypothesis testing - probability plotting techniques - Weibull - extreme value - hazard- binomial data - Analysis of load - strength interference - Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION- MODELLING AND DESIGN 9

Statistical design of experiments and analysis of variance Taguchi method - Reliability prediction - Reliability modeling - Block diagram and Fault tree Analysis - petric Nets - State space Analysis - Monte carlo simulation - Design analysis methods - quality function deployment - load strength analysis - failure modes - effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9

Reliability of electronic components - component types and failure mechanisms - Electronic system reliability prediction - Reliability in electronic system design - software errors - software structure and modularity - fault tolerance - software reliability - prediction and measurement - hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9

Test environments - testing for reliability and durability - failure reporting - Pareto analysis - Accelerated test data analysis - CUSUM charts - Exploratory data analysis and proportional hazards modeling - reliability demonstration - reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MAQNAGEMENT 9

Control of production variability - Acceptance sampling - Quality control and stress screening - Production failure reporting - preventive maintenance strategy - Maintenance schedules - Design for maintainability - Integrated reliability programmes - reliability and costs - standard for reliability - quality and safety - specifying reliability - organization for reliability.

Total: 45**TEXT BOOKS**

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, "Practical Reliability Engineering", 4th Edition, John Wiley & Sons, 2002.
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, "AT & T Reliability Manual", 5th Edition, New York, 1998.

REFERENCES

1. Gregg K. Hobbs, "Accelerated Reliability Engineering HALT and HASS", John Wiley & Sons, New York, 2000.
2. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.

AN5008 – INTERNETWORKING MULTIMEDIA

L	T	P
3	0	0

UNIT I MULTIMEDIA NETWORKING 9

Digital sound - video and graphics - basic multimedia networking - multimedia characteristics - evolution of Internet services model - network requirements for audio/ video transform - multimedia coding and compression for text image - audio and video.

UNIT II BROADBAND NETWORK TECHNOLOGY 9

Broadband services - ATM and IP - IPV6 - High speed switching - resource reservation - Buffer management - traffic shaping - caching – scheduling and policing – throughput - delay and jitter performance - Storage and media services - voice and video over IP - MPEG-2 over ATM/IP - indexing synchronization of requests - recording and remote control.

UNIT III RELIABLE TRANSPORT PROTOCOL AND APPLICATIONS 9

Multicast over shared media network - multicast routing and addressing - scaping multicast and NBMA networks - Reliable transport protocols - TCP adaptation algorithm – RTP – RTCP - MIME- Peer to Peer computing - shared application - video conferencing - centralized and distributed conference control - distributed virtual reality - light weight session philosophy.

UNIT IV MULTIMEDIA COMMUNICATION STANDARDS 9

Objective of MPEG - 7 standard - Functionalities and systems of MPEG - 7 – MPEG -21 Multimedia Framework Architecture - Content representation - Content Management and usage - Intellectual property management - Audio visual system - H322 - Guaranteed QOS LAN systems – MPEG - 4 video Transport across internet.

UNIT V MULTIMEDIA COMMUNICATION ACROSS NETWORKS 9

Packet Audio/video in the network environment - video transport across Generic networks - Layered video coding - error Resilient video coding techniques - Scalable Rate control - Streaming video across Internet - Multimedia transport across ATM networks and IP network - Multimedia across wireless networks.

Total: 45

TEXT BOOKS

1. Jon Crowcroft, Mark Handley, Ian Wakeman, “Internetworking Multimedia”,Harcourt Asia Pvt. Ltd. Singapore, 1998
2. K.R. Rao, Zoran S. Bojkovic and Dragorad A. Milovanovic, “Multimedia Communication systems”, PHI, 2003

REFERENCES

1. B.O. Szuprowicz, “Multimedia Networking”, McGraw Hill, 1995.
2. Tay Vaughan, “Multimedia making it to work”, 4th Edition, Tata McGraw Hill, 2000.

**AN5009 – ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN
SYSTEM DESIGN**

L T P
3 0 0

UNIT I EMI ENVIRONMENT 9

EMI/EMC concepts and definitions - Sources of EMI - conducted and radiated EMI - Transient EMI - Time domain Vs Frequency domain EMI - Units of measurement parameters - Emission and immunity concepts - ESD.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted - Radiated and Transient Coupling - Common Impedance Ground Coupling - Radiated Common Mode and Ground Loop Coupling - Radiated Differential Mode Coupling - Near Field Cable to Cable Coupling - Power Mains and Power Supply coupling.

UNIT III EMI/EMC STANDARDS AND MEASUREMENTS 9

Civilian standards - FCC - CISPR - IEC - EN - Military standards - MIL STD 461D/462 - EMI Test Instruments /Systems - EMI Shielded Chamber - Open Area Test Site - TEM Cell - Sensors/Injectors/Couplers - Test beds for ESD and EFT - Military Test Method and Procedures (462).

UNIT IV EMI CONTROL TECHNIQUES 9

Shielding – Filtering – Grounding – Bonding - Isolation Transformer - Transient Suppressors - Cable Routing - Signal Control - Component Selection and Mounting.

UNIT V EMC DESIGN OF PCBs 9

PCB Traces Cross Talk - Impedance Control - Power Distribution Decoupling – Zoning - Motherboard Designs and Propagation Delay Performance Models.

Total: 45

TEXT BOOKS

1. Henry W. Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, New York. 1988.
2. C.R. Paul, "Introduction to Electromagnetic Compatibility", John Wiley and Sons, Inc, 1992

REFERENCES

1. V.P. Kodali, "Engineering EMC Principles - Measurements and Technologies", IEEE Press, 1996.
2. Bernhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Edition, Artech house, 1986.

CO5001 – RF SYSTEM DESIGN

L T P
3 0 0

UNIT I RF ISSUES 9

Importance of RF design - Electromagnetic Spectrum - RF behaviour of passive components - Chip components and Circuit Board considerations - Scattering Parameters - Smith Chart and applications

UNIT II RF FILTER DESIGN 9

Overview - Basic resonator and filter configuration - Special filter realizations - Filter implementations - Coupled filter.

UNIT III ACTIVE RF COMPONENTS & APPLICATIONS 9

RF diodes - BJT - RF FETs - High electron mobility transistors - Matching and Biasing Networks - Impedance matching using discrete components - Microstripline matching networks - Amplifier classes of operation and biasing networks.

UNIT IV RF AMPLIFIER DESIGNS 9

Characteristics - Amplifier power relations - Stability considerations - Constant gain circles - Constant VSWR circles - Low Noise circuits - Broadband - high power and multistage amplifiers.

UNIT V OSCILLATORS - MIXERS & APPLICATIONS 9

Basic Oscillator model - High frequency oscillator configuration - Basic characteristics of Mixers - Phase Locked Loops - RF directional couplers and hybrid couplers - Detector and demodulator circuits

Total: 45

TEXT BOOK

1. Reinhold Ludwig and Powel Bretchko, "RF Circuit Design Theory and Applications", 1st Edition, Pearson Education Asia, 2001.
2. Mathew M. Radmanesh, "Radio Frequency & Microwave Electronics", Second Edition Pearson Education Asia, 2002.

REFERENCES

1. Joseph J. Carr, "Secrets of RF Circuit Design", Third Edition, McGraw Hill Publishers, 2000.
2. Ulrich L. Rohde and David P. NewKirk, "RF / Microwave Circuit Design", John Wiley & Sons, USA, 2000.
3. Roland E. Best, "Phase Locked Loops, Design, simulation and applications", 5th Edition, McGraw Hill Publishers, 2003.

VL5002 – LOW POWER VLSI DESIGN

L	T	P
3	0	0

UNIT I	POWER DISSIPATION IN CMOS	9
Hierarchy of limits of power - Sources of power consumption - Physics of power dissipation in CMOS FET devices - Basic principle of low power design.		
UNIT II	POWER OPTIMIZATION	9
Logical level power optimization - Circuit level low power design - Circuit techniques for reducing power consumption in adders and multipliers.		
UNIT III	DESIGN OF LOW POWER CMOS CIRCUITS	9
Computer Arithmetic techniques for low power systems - Reducing power consumption in memories - Low power clock- Interconnect and layout design - Advanced techniques - Special techniques		
UNIT IV	POWER ESTIMATION	9
Power estimation techniques - Logic level power estimation - Simulation power analysis - Probabilistic power analysis.		
UNIT V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER	9
Synthesis for low power - Behavioral level transforms - Software design for low power		

Total: 45

TEXT BOOKS

1. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
2. K. Roy and S.C. Prasad, "Low Power CMOS VLSI circuit design", Wiley, 2000.

REFERENCES

1. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for low power", Kluwer, 2002.
2. J.B. Kuo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
3. A.P. Chandrakasan and R.W. Broadersen, "Low power digital CMOS design", Kluwer, 1995.
4. Abdellatif Bellaouar, Mohamed. I. Elmasry, "Low power digital VLSI designs"Kluwer, 1995.

UNIT I FUNDAMENTALS TO DSP SYSTEMS 9

Introduction to DSP Systems - Typical DSP algorithms - Iteration Bound - data flow graph representations - loop bound and iteration bound - Longest path Matrix algorithm - Pipelining and parallel processing - Pipelining of FIR digital filters - parallel processing - pipelining and parallel processing for low power.

UNIT II RETIMING 9

Retiming - definitions and properties - Unfolding - an algorithm for Unfolding - properties of unfolding - sample period reduction and parallel processing application - Algorithmic strength reduction in filters and transforms - 2-parallel FIR filter - 2-parallel fast FIR filter - DCT algorithm architecture transformation - parallel architectures for rank - order filters – Odd, Even - Merge Sort architecture - parallel rankorder filters.

UNIT III FAST CONVOLUTION 9

Fast convolution - Cook-Toom algorithm - modified Cook - Took algorithm - Pipelined and parallel recursive and adaptive filters - inefficient/efficient single channel interleaving - Look Ahead pipelining in first order IIR filters – Look Ahead pipelining with power of two decomposition - Clustered Look - Ahead pipelining- parallel processing of IIR filters - combined pipelining and parallel processing of IIR filters - pipelined adaptive digital filters - relaxed look ahead - pipelined LMS adaptive filter.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and roundoff noise - scaling operation - roundoff noise - state variable description of digital filters - scaling and roundoff noise computation - roundoff noise in pipelined firstorder filters – Bit Level Arithmetic Architectures - parallel multipliers with sign extension - parallel carry ripple array multipliers - parallel carry save multiplier - 4x4 bit Baugh - Wooley carry save multiplication tabular form and implementation- design of Lyon’s bit-serial multipliers using Horner’s rule- bit-serial FIR filter - CSD representation - CSD multiplication using Horner’s rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Numerical Strength Reduction - sub expression elimination - multiple constant multiplications - iterative matching - Linear transformations - Synchronous - Wave and asynchronous pipelining - synchronous pipelining and clocking styles - clock skew in edge triggered single phase clocking – two phase clocking - wave pipelining - asynchronous pipelining bundled data versus dual rail protocol - Programming Digital Signal Processors - general architecture with important features - Low power Design - needs for low power VLSI chips - charging and discharging capacitance - short-circuit current of an inverter - CMOS leakage current basic principles of low power design.

Total: 45

TEXT BOOK

1. Keshab K. Parhi, “VLSI Digital Signal Processing systems Design and implementation”, Wiley, Inter Science, 1999.

REFERENCES

1. Mohammed Isamail and Terri Fiez, “Analog VLSI Signal and Information Processing”, Mc Graw Hill, 1994.
2. Y. Kung, H.J. White House, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
3. Jose E. France, Yannis Tsvividis, “Design of Analog Digital VLSI Circuits for Telecommunication and Signal Processing”, Prentice Hall, 1994.

VL5005 – ANALOG VLSI DESIGN

L T P
3 0 0

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING 9

Mixed Signal VLSI Chips - Basic CMOS Circuits - Basic Gain Stage - Gain Boosting Techniques - Super MOS Transistor - Primitive Analog Cells - Linear Voltage - Current Converters - MOS Multipliers and Resistors – CMOS Bipolar and Low Voltage BiCMOS Op-Amp Design - Instrumentation Amplifier Design - Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous Time Signal Processing - Sampled Data Signal Processing - Switched-Current Data Converters - Practical Considerations in SI Circuits Biologically - Inspired Neural Networks - Floating - Gate- Low Power Neural Networks - CMOS Technology and Models - Design Methodology – Networks - Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First order and Second SC Circuits - Bilinear Transformation - Cascade Design - Switched - Capacitor Ladder Filter - Synthesis of Switched - Current Filter - Nyquist rate A/D Converters - Modulators for Over sampled A/D Conversion - First and Second Order and Multibit Sigma - Delta Modulators - Interpolative Modulators - Cascaded Architecture - Decimation Filters - mechanical - Thermal - Humidity and Magnetic Sensors - Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modelling and Simulation - Testability - Analysis Technique - Ad Hoc Methods and General Guidelines - Scan Techniques - Boundary Scan Built-in Self Test - Analog Test Buses - Design for Electron - Beam Testability - Physics of Interconnects in VLSI Scaling of Interconnects - A Model for Estimating Wiring Density - A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG DIGITAL LAYOUT 9

Review of Statistical Concepts - Statistical Device Modeling - Statistical Circuit Simulation - Automation Analog Circuit Design - automatic Analog Layout - CMOS Transistor Layout - Resistor Layout - Capacitor Layout - Analog Cell Layout - Mixed Analog - Digital Layout.

Total: 45

TEXT BOOKS

1. Mohammed Ismail, Terri Fiez, "Analog VLSI signal and Information Processing", McGraw Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C. May, "Analog VLSI Design NMOS and CMOS ", Prentice Hall, 1998.

REFERENCES

1. Randall L Geiger, Phillip E. Allen, Noel K. Strader, "VLSI Design Techniques forAnalog and Digital Circuits", Mc Graw Hill International Company, 1990.
2. Jose E. France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits forTelecommunication and signal processing", Prentice Hall, 1994.

VL5151 – COMPUTER AIDED DESIGN OF VLSI CIRCUITS

L	T	P
3	0	0

UNIT I VLSI FUNDAMENTALS 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II TOPOLOGY RULES AND ALGORITHMS 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING AND ROUTING 9

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV MODULING AND SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V SCHEDULING AND ALGORITHMS 9

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

Total: 45

TEXT BOOKS

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.

REFERENCES

1. Drechsler, R. "Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers, 1998.
2. Hill D., D. Shugard, J. Fishburn and K. Keutzer, "Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Academic Publishers, 1989.