ANNA UNIVERSITY TIRUCHIRAPPALLI
Tiruchirappalli – 620 024

Curriculum

M.E. EMBEDDED SYSTEM TECHNOLOGIES

SEMESTER I

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**MA5145**	Applied Mathematics for Embedded System	3	1	0	4
2	**AN5102**	Advanced Digital System Design	3	0	0	3
3	**ES5101**	Micro Controller System Design and Applications	3	0	0	3
4	**ES5102**	Software Technology for Embedded Systems	3	0	0	3
5	**ES5103**	Real Time Systems	3	0	0	3
6	**E1******	Elective I	3	0	0	3
					Total	**19**

SEMESTER II

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**ES5151**	Real Time Operating System	3	0	0	3
2	**ES5152**	Embedded Networking	3	0	0	3
3	**ES5153**	VLSI Architecture and Design Methodologies	3	1	0	4
4	**ES5154**	Design of Embedded Systems	3	0	0	3
5	**E2*****	Elective II	3	0	0	3
6	**E2*****	Elective III	3	0	0	3
Practical						
7	**ES5155**	Embedded System Laboratory	0	0	2	2
					Total	**21**

SEMESTER III

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**E4*** **	Elective IV	3	0	0	3
2	**E5*** **	Elective V	3	0	0	3
3	**E6*** **	Elective VI	3	0	0	3
Practical						
4	**ES5251**	Project Work - Phase I	0	0	12	6
					Total	**15**

SEMESTER IV

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**ES5251**	Project Work - Phase II	0	0	24	12
					Total	**12**

LIST OF ELECTIVES

S.No.	Subject Code	Subject	L	T	P	C
Theory						
1	**ES5001**	Embedded Control Systems	3	0	0	3
2	**ES5002**	Cryptography and Network Security	3	0	0	3
3	**ES5003**	Digital Image Processing	3	0	0	3
4	**ES5004**	Operating Systems	3	0	0	3
5	**ES5005**	Computer Architecture	3	0	0	3
6	**ES5006**	Wireless and Mobile Communication	3	0	0	3
7	**ES5007**	Advanced Embedded Systems	3	0	0	3
8	**ES5008**	VHDL	3	0	0	3
9	**ES5009**	Data Communication and Networks	3	0	0	3
10	**ES5010**	Multimedia Systems	3	0	0	3
11	**AN5005**	ASIC Design	3	0	0	3
12	**ES5011**	Advanced Microprocessors and Micro controllers Design	3	0	0	3
13	**ES5012**	Embedded Communication Software Design	3	0	0	3
14	**ES5013**	DSP Integrated Circuits	3	0	0	3
15	**CI5102**	Digital Signal Processing	3	0	0	3

ANNA UNIVERSITY TIRUCHIRAPPALLI
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Regulations 2008

Syllabus

M.E. EMBEDDED SYSTEM TECHNOLOGIES

SEMESTER I

MA5145 – APPLIED MATHEMATICS FOR EMBEDDED SYSTEMS

L	T	P	C
3	1	0	4

UNIT I THE WAVE EQUATION 9

Solution of initial and boundary value problems – Characteristics – D'Alembert's Solution – Significance of Characteristic curves – Laplace transform solutions for displacement in a long string – a long string under its weight – a bar with prescribed force on one end – free vibration of a string.

UNIT II SPECIAL FUNCTIONS 9

Series solutions – Bessel's equation – Bessel Functions – Legendre's equation – Legendre Polynomials – Rodrigue's formula – Recurrence relations – Generating Functions and orthogonal property for Bessel functions of the first kind – Legendre Polynomials.

UNIT III FOURIER ANALYSIS AND Z –TRANSFORMS 9

Discrete Fourier Transforms and its properties – Fourier series and its properties – Fourier representation of finite duration sequences – Z-transform – Properties of the region of convergence – Inverse Z-transform – Z-transform properties.

UNIT IV PROBABILITY AND RANDOM VARIABLES 9

Probability – Random variables – Binomial, Poisson, Geometric, Uniform, Normal, Exponential distributions – Moment generating functions and their properties – Functions of Random variables.

UNIT V QUEUEING THEORY 9

Single and Multiple server Markovian Queuing models – Customer impatience – Queuing applications.

L: 45 T: 15 Total: 60

TEXT BOOKS

1. Andrews L.C., and Shivamoggi, B.K. Integral Transforms for Engineers, Prentice Hall of India Pvt. Ltd, New Delhi, 2003.
2. Gupta, S.C and Kapoor V.K., Fundamentals of Mathematical Statistics, Sultan Chand and sons, New Delhi, 2001.
3. Taha H .A., Operations Research: An Introduction, Pearson Education Edition, Asia, New Delhi, Seventh Edition 2002.
4. O'Neil P.V., Advanced Engineering Mathematics, Thomson Brooks/Cole, Singapore, 5th Edition, 2003.
5. Andrews L.C., Special Functions of Mathematics for Engineers, McGraw Hill, Inc., Singapore, 2nd Edition, 1992.

REFERENCES

1. Sankara Rao K., Introduction to Partial Equations, Prentice Hall of India Pvt. Ltd., New Delhi, 1997.
2. Sneddon I.N, The use of Integral Transforms, McGraw Hill Book Co, NewYork, 1972.
3. Churchill R.V., Operational Mathematics, McGraw Hill Kogakusha Ltd, Tokyo, 1981.
4. S.Narayanan, T.K.Manickavachagam Pillay and G.Ramaniah, Advanced Mathematics for Engineering Students Vol.II, S.Viswanathan Pvt. Ltd., 1986.
5. Walpole R.E., Myer R.H., Myer S.L., and Ye, K., Probability and Statistics for Engineers and Scientists, Pearson Education, 7th Edition, Delhi, 2002.
6. Goel, B.S., and Mittal, S.K. Operations Research, Pragati Prakashan, Meerut, 2000.

AN5102 – ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

UNIT V SYSTEM DESIGN USING VHDL 9

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modelling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

Total: 45

REFERENCES

1. Donald G. Givone "Digital principles and Design" Tata McGraw Hill 2002.
2. John M Yarbrough "Digital Logic applications and Design" Thomson Learning, 2001
3. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001
4. Charles H. Roth Jr. "Digital System Design using VHDL" Thomson Learning, 1998.
5. Charles H. Roth Jr. "Fundamentals of Logic design" Thomson Learning, 2004.
6. Stephen Brown and Zvonk Vranesic "Fundamentals of Digital Logic with VHDL Deisgn" Tata McGraw Hill, 2002.
7. Navabi.Z. "VHDL Analysis and Modeling of Digital Systems. McGraw International, 1998.
8. Parag K Lala, "Digital System design using PLD" BS Publications, 2003
9. Peter J Ashendem, "The Designers Guide to VHDL" Harcourt India Pvt Ltd, 2002
10. Mark Zwolinski, "Digital System Design with VHDL" Pearson Education, 2004
11. Skahill. K, "VHDL for Programmable Logic" Pearson education, 1996.

ES5101 – MICROCONTROLLER SYSTEM DESIGN AND APPLICATIONS

L	T	P	C
3	1	0	3

UNIT I 8051 ARCHITECTURE 9

Basic organization – 8051 CPU structure – Register file – Interrupts – Timers – Port circuits – Instruction set – Timing diagram – Addressing modes – Simple Program and Applications.

UNIT II PERIPHERALS AND INTERFACING 9

Typical Bus structure – Bus – memory organization – Timing characteristics – Extended Model and Memory Interfacing – Polling – Interfacing Basic I/O devices – Analog and Digital interfacing – PWM mode operation – Serial port application.

UNIT III 8096 ARCHITECTURE 9

CPU operation – Interrupt structure – Timers – High Speed Input / Output Ports – I/O control and Status registers – Instruction Set – Addressing Modes – Simple Programming – Queues – Tables and Strings – Stack Memories – Key Switch – Parsing.

UNIT IV PERIPHERALS AND INTERFACING 9

Analog Interface – Serial Ports – Watch dog timers – Real Time Clock – Multitasking – Bus Control – Memory Timing – External ROM and RAM expansion – PWM control – A/D interfacing.

UNIT V CASE STUDY FOR 8051 AND 8096 9

Real Time clock – DC Motor Speed Control – Generation of Gating Signals for Converters and Inverters – Frequency Measurement – Temperature Control

Total: 45

REFERENCES

1. John B.Peatman, “Design with Micro controllers”, McGraw Hill international Limited Singapore, 1989.
2. Michael Slater, “Microprocessor based design A comprehensive guide to effective Hardware design” Prentice Hall, New Jersey, 1989.
3. Ayala, Kenneth, “The 8051 Microcontroller” Upper Saddle River, New Jersey PrenticeHall, 2000.
4. Intel manual on 16 bit embedded controllers, Santa Clara, 1991.
5. Muhammad Ali Mazidi, Janice Gillispie mazidi. “The 8051 Microcontroller and Embedded systems”, Person Education, 2004.

ES5102 – SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

UNIT I PROGRAMMING EMBEDDED SYSTEMS 9

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Toper of memory – Memory testing – Flash Memory.

UNIT II OPERATING SYSTEM 9

Embedded operating system – Real time characteristics – Selection process – Flashing the LED – serial ports – Zilog 85230 serial controlled code efficiency – Code size – Reducing memory usage – Impact of C++.

UNIT III PROCESSOR ARCHITECTURE 9

Hardware fundamentals – Buses – DMA – interrupts – Built-ins on the microprocessor – Conventions used on schematics – Microprocessor Architectures – Software Architectures – RTOS Architectures – Selecting an Architecture.

UNIT IV RTOS CONCEPTS 9

RTOS – Tasks and Task states – Semaphores – Shared data – Message queues, Mail boxes and pipes – Memory management – Interrupt routines – Encapsulating semaphore and queues – Hard Real-time scheduling – Power saving.

UNIT V EMBEDDED TOOLS 9

Embedded Software development tools – Host and target machines – Linkers / Locators for Embedded Software – Debugging techniques – Instruction set simulators Laboratory tools – Practical example – Source code.

Total: 45

REFERENCES

1. David E.Simon: An Embedded Software Primer Perason Education, 2003.
2. Michael Bass: Programming Embedded Systems in C and C++ Oreilly, 2003.

ES5103 – REAL TIME SYSTEMS

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION 9

Introduction – Issues in Real Time Computing, Structure of a Real Time System, Task classes, Performance Measures for Real Time Systems, Estimating Program Run Times. Task Assignment and Scheduling – Classical uniprocessor scheduling algorithms, Uniprocessor scheduling of IRIS tasks, Task assignment, Mode changes, and Fault Tolerant Scheduling.

UNIT II PROGRAMMING LANGUAGES AND TOOLS 9

Programming Languages and Tools – Desired language characteristics, Data typing, Control structures, Facilitating Hierarchical Decomposition, Packages, Run – time (Exception) Error handling, Overloading and Generics, Multitasking, Low level programming, Task Scheduling, Timing Specifications, Programming Environments, Run – time support**.**

UNIT III REAL TIME DATABASES 9

Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability, Maintaining Serialization Consistency, Databases for Hard Real Time Systems.

UNIT IV COMMUNICATION 9

Real – Time Communication – Communications media, Network Topologies Protocols, Fault Tolerant Routing. Fault Tolerance Techniques – Fault Types, Fault Detection. Fault Error containment Redundancy, Data Diversity, Reversal Checks, Integrated Failure handling.

UNIT V EVALUATION TECHNIQUES 9

Reliability Evaluation Techniques – Obtaining parameter values, Reliability models for Hardware Redundancy, Software error models. Clock Synchronization – Clock, A Nonfault – Tolerant Synchronization Algorithm, Impact of faults, Fault Tolerant Synchronization in Hardware, Fault Tolerant Synchronization in software.

Total: 45

TEXT BOOK

1. C.M. Krishna, Kang G. Shin, “Real – Time Systems”, McGraw – Hill International Editions, 1997.

REFERENCES

1. Stuart Bennett, “Real Time Computer Control – An Introduction”, Prentice Hall of India, 1998.
2. Peter D.Lawrence, “Real Time Micro Computer System Design – An Introduction”, McGraw Hill, 1988.
3. S.T. Allworth and R.N.Zobel, “Introduction to real time software design”, Macmillan, 2nd Edition, 1987.
4. R.J.A Buhur, D.L Bailey, “An Introduction to Real – Time Systems”, Prentice – Hall International, 1999.
5. Philip.A.Laplante, “Real Time System Design and Analysis”, Prentice Hall of India, 3rd Edition, April 2004.

SEMESTER II

ES5151 – REAL TIME OPERATING SYSTEMS

L	T	P	C
3	0	0	3

UNIT I REVIEW OF OPERATING SYSTEMS 9

Basic Principles – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Operating System structures.

UNIT II DISTRIBUTED OPERATING SYSTEMS 9

Topology – Network types – Communication – RPC – Client server model – Distributed file system – Design strategies.

UNIT III REAL TIME MODELS AND LANGUAGES 9

Event Based – Process Based and Graph based Models – Petrinet Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT IV REAL TIME KERNEL 9

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V RTOS APPLICATION DOMAINS 9

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

Total: 45

REFERENCES

1. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
2. Charles Crowley, “Operating Systems-A Design Oriented approach” McGraw Hill 1997.
3. C.M. Krishna, Kang, G.Shin, “Real Time Systems”, McGraw Hill, 1997.
4. Raymond J.A.Bhur, Donald L.Bailey, “An Introduction to Real Time Systems”, PHI 1999.

ES5152 – EMBEDDED NETWORKING

L	T	P	C
3	0	0	3

UNIT I EMBEDDED NETWORK REQUIREMENTS 9

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

UNIT II CAN OPEN CONFIGURATION 9

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

UNIT III OVERVIEW OF CAN 9

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

UNIT IV IMPLEMENTATION OF CAN 9

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code – Conformance test – Entire design life cycle.

UNIT V ISSUES AND EMERGING TRENDS IN CAN 9

Implementation issues – Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

Total: 45

TEXT BOOK

1. Glaf P.Feiffer, Andrew Ayre and Christian Keyold “Embedded Networking with CAN and CAN open”. Embedded System Academy 2005.

ES5153 – VLSI ARCHITECTURE AND DESIGN METHODOLOGIES

L	T	P	C
3	1	0	4

UNIT I INTRODUCTION 9

Overview of digital VLSI design methodologies – Trends in IC Technology – Advanced Boolean algebra – Shannon's expansion theorem – Consensus theorem – Octal designation- Run measure – Buffer gates - Gate expander – Reed Muller expansion – Synthesis of multiple output combinational logic circuits by product map method – Design of static hazard free, dynamic hazard free logic circuits.

UNIT II NALOG VLSI AND HIGH SPEED VLSI 9

Introduction to analog VLSI – realization of neural networks and switched capacitor filters – Sub-micron technology and Gas VLSI Technology.

UNIT III PROGRAMMABLE ASICS 9

Anti fuse – static RAM – EPROM and technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera flex – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

UNIT IV PROGRAMMABLE ASIC DESIGN SOFTWARE 9

Actel ACT – Xilinux LCA – Xilinux EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – design systems – logic synthesis – half gate – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

UNIT V LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Basic features of VHDL language for behavioral modeling and simulation – Summary of VHDL data types – Dataflow and structural modeling – VHDL and logic synthesis – Circuit and layout verification – Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation – design examples.

L: 45 T: 15 Total: 60

REFERENCES

1. William I.Fletcher, "An Engineering Approach to Digital Design", Prentice Hall of India.
2. Amar Mukharjee, "Introduction to NMOS and CMOS VLSI System Design", Prentice Hall, 1986.
3. M.J.S. Smith, "Application – specific integrates circuits", Addison Wesley Longman Inc. 1997.
4. Frederick J.Hill and Gerald R.Peterson, "Computer Aided Logical Design with emphasis on VLSI".

ES5154 – DESIGN OF EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

UNIT I **9**

Embedded Design life cycle – Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other issues in selection processes.

UNIT II **9**

Partitioning decision – Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System startup – Hardware manipulation – memory – mapped access – speed and code density.

UNIT III **9**

Interrupt Service routines – Watch dog timers – Flash memory Basic toolset – Host ased debugging – Remote debugging – ROM emulators – logic Analyzer – Caches – Computer optimisation – Statistical profiling.

UNIT IV **9**

In circuit emulators – Buller proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

UNIT V **9**

Testing – Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

Total: 45

REFERENCE

1. Arnold S. Berger – Embedded System Design CMP books, USA 2002.

ES5155 – EMBEDDED SYSTEMS LABORATORY

L	T	P	C
0	0	2	2

1. Micro controller 8051/8031 & Flash controller programming
   a) Simple application programs with kit and through assembler
   b) Data flash with erase, verify, fusing through ATMEL and INTEL tools.

2. Testing RTOS Environment and System Programming.
   a) Keil Tools
   b) RTOS System Solutions with Tornado tools.

3. Complex Programmable Logic Devices and Device Programming with VHDL fitter and Cool runner
   a) Warp tools-Cypress-Active HDL Simulator & Galaxy-VHDL, FSM models
   b) Mixed signal handling.

4. Third party design tools
   a) Mentor Graphics
   b) Cadence.

5. VLSI designing with various Tools and Design methodologies
   a) AT40K FPGA series-synthesis-design-simulation of application programs.
   b) Xilinx EDA design tools-device programming –PROM programming.
   c) ALTERA and Mentor graphics-IC design tools.

6. Embedded DSP based System Designing.
   a) Code compressor studio for embedded DSP using Texas tool kit.
   b) Analog DSP tool kit.

7. IPCORE usage in VOIP Through SoC2 tools
   a) Cypress PsoC designing Tools
   b) SoPC designing Tools

8. FPSLIC synthesis, Designing and Testing and BLUE TOOTH wireless Communication Designing.
   a) ATMEL FPSLIC tools
   b) CYPRESS BLUE TOOTH tools.

LIST OF ELECTIVES

ES5001 – EMBEDDED CONTROL SYSTEMS

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION 9

Controlling the hardware with software – Data lines – Address lines - Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

UNIT II INPUT-OUTPUT DEVICES 9

Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules – LCD module display – Configuration – Time-of-day clock – Timer manager - Interrupts - Interrupt service routines – IRQ - ISR - Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

UNIT III D/A AND A/D CONVERSION 9

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

UNIT IV ASYNCHRONOUS SERIAL COMMUNICATION 9

Asynchronous serial communication – RS-232 – RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module - Buffered serial I/O.

UNIT V CASE STUDIES: EMBEDDED C PROGRAMMING 9

Multiple closure problems – Basic outputs with PPI – Controlling motors – Bi-directional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

Total: 45

REFERENCES

1. Jean J. Labrosse, “Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C”, The publisher, Paul Temme, 1999.
2. Ball S.R., ‘Embedded microprocessor Systems – Real World Design’, Prentice Hall, 1996.
3. Herma K, “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
4. Daniel W. Lewis, “Fundamentals of Embedded Software where C and Assembly meet”, PHI, 2002.

ES5002 – CRYPTOGRAPHY AND NETWORK SECURITY

L	T	P	C
3	0	0	3

UNIT I SYMMETRIC CIPHERS 9

Overview – classical Encryption Techniques – Block Ciphers and the Data Encryption standard – Introduction to Finite Fields – Advanced Encryption standard – Contemporary Symmetric Ciphers – Confidentiality using Symmetric Encryption.

UNIT II PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS 9

Introduction to Number Theory – Public-Key Cryptography and RSA – Key Management – Diffie-Hellman Key Exchange – Elliptic Curve Cryptography – Message Authentication and Hash Functions – Hash Algorithms – Digital Signatures and Authentication Protocols.

UNIT III NETWORK SECURITY PRACTICE 9

Authentication Applications – Kerbors – X.509 Authentication Service – Electronic mail Security – Pretty Good Privacy – S/MIME – IP Security architecture – Authentication Header – Encapsulating Security Payload – Key Management.

UNIT IV SYSTEM SECURITY 9

Intruders – Intrusion Detection – Password Management – Malicious Software – Firewalls – Firewall Design Principles – Trusted Systems.

UNIT V WIRELESS SECURITY 9

Introduction to Wireless LAN Security Standards – Wireless LAN Security Factors and Issues.

Total: 45

TEXT BOOK

1. William Stallings, “Cryptography And Network Security – Principles And Practices”, Pearson Education, 3rd Edition, 2003.

REFERENCES

1. Atul Kahate, “Cryptography and Network Security”, Tata McGraw Hill, 2003.
2. Bruce Schneier, “Applied Cryptography”, John Wiley and Sons Inc, 2001.
3. Stewart S. Miller, “Wi-Fi Security”, McGraw Hill, 2003.
4. Charles B. Pfleeger, Shari Lawrence Pfleeger, “Security In Computing”, 3rd Edition, Pearson Education, 2003.
5. Mai, “Modern Cryptography: Theory and Practice”, First Edition, Pearson Education, 2003.

ES5003 – DIGITAL IMAGE PROCESSING

L	T	P	C
3	0	0	3

UNIT I FUNDAMENTALS OF IMAGE PROCESSING 9

Introduction – Steps in image processing systems – Image acquisition – Sampling and Quantization – Pixel relationships – Color fundamentals and models, File formats, Image operations – Arithmetic, Geometric and Morphological.

UNIT II IMAGE ENHANCEMENT 9

Spatial Domain: Gray level Transformations – Histogram processing – Spatial filtering smoothing and sharpening. Frequency Domain: Filtering in frequency domain – DFT, FFT, DCT – Smoothing and sharpening filters – Homomorphic Filtering.

UNIT III IMAGE SEGMENTATION AND FEATURE ANALYSIS 9

Detection of Discontinuities – Edge operators – Edge linking and Boundary Detection – Thresholding – Region based segmentation – Morphological Watersheds – Motion Segmentation, Feature Analysis and Extraction.

UNIT IV MULTI RESOLUTION ANALYSIS AND COMPRESSIONS 9

Multi Resolution Analysis: Image Pyramids – Multi resolution expansion – Wavelet Transforms. Image compression: Fundamentals – Models – Elements of Information Theory – Error free compression – Lossy Compression – Compression Standards.

UNIT V APPLICATIONS OF IMAGE PROCESSING 9

Image classification – Image recognition – Image understanding – Video motion analysis – Image fusion – Steganography – Digital compositing – Mosaics – Colour Image Processing.

Total: 45

REFERENCES

1. Rafael C. Gonzalez and Richard E. Woods, “Digital Image Processing”, 2nd Edition, Pearson Eduction, 2003.
2. Milan Sonka, Vaclav Hlavac and Roger Boyle, “Image Processing, Analysis and Machine Vision ”, 2nd Edition, Thomson Learning, 2001.
3. Anil K. Jain, “Fundamentals of Digital Image Processing”, Pearson Education, 2003.

ES5004 – OPERATING SYSTEMS

L	T	P	C
3	0	0	3

UNIT I **9**

Introduction – Operating systems and services – Processes – CPU Scheduling approaches.

UNIT II **9**

Process synchronization – Semaphores – Deadlocks – Handling deadlocks – Multithreading.

UNIT III **9**

Memory management – Paging – Segmentation – Virtual memory – Demand paging – Replacement algorithms.

UNIT IV **9**

Disk Scheduling approaches – File systems – Design issues – User interfaces to file systems – I / O device management.

UNIT V **9**

Case study – Design and implementation of the UNIX OS, process model and Structure – Memory management – File system – UNIX I / O management and Device drivers – Windows – System components – Process management – Memory management – File systems – Networking.

Total: 45

REFERENCES

1. Abraham Silberschatz Peter B. Galvin, G.Gagne, “Operating System Concepts”, 6th Edition, Wesley Publishing company, 2003.
2. M.J.Bach, Design of the UNIX Operating System, Prentice Hall, 1986.

ES5005 – COMPUTER ARCHITECTURE

L	T	P	C
3	0	0	3

UNIT I FUNDAMENTALS OF COMPUTER DESIGN 9

Review of fundamentals of CPU, Memory and IO – Performance evaluation – Instruction set principles – Design issues – Example Architectures.

UNIT II INSTRUCTION LEVEL PARALLELISM 9

Pipelining and handling hazards – Dynamic Scheduling – Dynamic hardware prediction – Multiple issue – Hardware based speculation – Limitations of ILP – Case studies.

UNIT III INSTRUCTION LEVEL PARALLELISM WITH SOFTWARE APPROACHES 9

Compiler techniques for exposing ILP – Static branch prediction – VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism - Hardware versus software speculation mechanisms – IA 64 and ltanium processor.

UNIT IV MEMORY AND I/O 9

Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.

UNIT V MULTIPROCESSORS AND THREAD LEVEL PARALLELISM 9

Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Multithreading.

Total: 45

REFERENCES

1. John L.Hennessey and David A.Patterson, “Computer Architecture: A Quantitative Approach”, Third Edition, Morgan Kaufmann, 2003.
2. D.Sia, T.Fountain and P.Kacsuk, “Advanced computer Architectures: A Design Space Approach”, Addion Wesley, 2000.

ES5006 – WIRELESS AND MOBILE COMMUNICATION

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION 9

Wireless Transmission-signal propagation-spread spectrum-Satellite Networks-Capacity Allocation-FAMA-DAMA-MAC

UNIT II MOBILE NETWORKS 9

Cellular Wireless Networks-GSM-Architecture-Protocols-Connection Establishment-Frequently Allocation-Routing-Handover-Security-GPRA

UNIT III WIRELESS NETWORKS 9

Wireless LAN-IEEE 802.11 Standard-Architecture-Services-AdHoc Network-HiperLan-Blue Tooth

UNIT IV ROUTING 9

Mobile IP-DHCP- AdHoc Networks-Proactive and Reactive Routing Protocols-Multicast Routing

UNIT V TRANSPORT AND APPLICATION LAYERS 9

TCP over Adhoc Networks-WAP-Architecture-WWW Programming Model-WDP -WTLS-WTP-WSP-WAE-WTA Architecture-WML-WML scripts

Total: 45

REFERENCES

1. Kaveh Pahlavan, Prasanth Krishnamoorthy, " Principles of Wireless Networks' PHI/Pearson Education, 2003
2. Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, " Principles of Mobile computing", Springer, New york, 2003.
3. C.K.Toh, " AdHoc mobile wireless networks", Prentice Hall, Inc, 2002.
4. Charles E. Perkins, " Adhoc Networking", Addison-Wesley, 2001.
5. Jochen Schiller, " Mobile communications", PHI/Pearson Education, Second Edition, 2003.
6. William Stallings, " Wireless communications and Networks", PHI/Pearson Education, 2002.

ES5007 – ADVANCED EMBEDDED SYSTEMS

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UNIT I INTRODUCTION AND REVIEW OF EMBEDDED HARDWARE 9

Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Round-Robin – Round Robin with interrupt function – Rescheduling architecture – algorithm.

UNIT II REAL TIME OPERATING SYSTEM 9

Task and Task states – Task and data – Semaphore and shared data operating system services – Message queues timing functions – Events – Memory management – Interrupt routines in an RTOS environment – Basic design using RTOS.

UNIT III EMBEDDED HARDWARE, SOFTWARE AND PERIPHERALS 9

Custom single purpose processors: Hardware – Combination Sequence – Processor design – RT level design – optimising software: Basic Architecture – Operation – Programmers view – Development Environment – ASIP – Processor Design – Peripherals – Timers, counters and watch dog timers – UART – Pulse width modulator – LCD controllers – Key pad controllers – Stepper motor controllers – A/D converters – Real time clock.

UNIT IV MEMORY AND INTERFACING 9

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example.

UNIT V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO-DESIGN 9

Modes of operation – Finite state machines – Models – HCFSL and state charts language – state machine models – Concurrent process model – Concurrent process – Communication among process –Synchronization among process – Implementation – Data Flow model. Design technology; Automation synthesis – Hardware software co-simulation – IP cores – Design Process Model.

Total: 45

REFERENCES

1. David. E.Simon “An Embedded Software Primer”, Pearson Education, 2001.
2. Frank Vahid and Tony Gwargie “Embedded System Design”, John Wiley & sons, 2002.
3. Steve Heath, “Embedded System Design”, Elserien, Second Edition, 2004.

ES5008 – VHDL

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UNIT I VHDL FUNDAMENTALS 9

Fundamental Concepts – Modeling Digital Systems – Domains and Levels of Modeling – Modeling Languages – VHDL Modeling concepts – Scalar Data Types and Operations – Constants and variables – Scalar Types – Type Classification – Attributes and Scalar types – Expressions and operators – Sequential Statements – If statements – Case statements – Null Statements – Loop statements – Assertion and Report statements.

UNIT II COMPOSITE DATA TYPES AND BASIC MODELING CONSTRUCTS 9

Arrays – Unconstrained Array types – Array Operations and Referencing – Records – Basic Modeling Constructs – Entity Declarations – Architecture Bodies – Behavioral Descriptions – Structural Descriptions – Design Processing.
Case Study: A pipelined Multiplier Accumulator.

UNIT III SUBPROGRAMS AND PACKAGES 9

Procedures – Procedure Parameters – Concurrent Procedure Call Statements – functions – Overloading – Visibility of Declarations – Packages and Use Clauses – Package declarations – Package bodies – Use Clauses – The predefined – Aliases - Aliases for data objects – Aliases for Non-Data Items.
Case Study: A Bit-Vector Arithmetic Package.

UNIT IV SIGNALS, COMPONENTS, CONFIGURATIONS 9

Basic Resolved signals – IEEE Std_Logic_1164 Resolved subtypes – Resolved signal parameters – Generic Constants – Parameterizing behavior – Parameterizing structure – Components and Configurations – Components – Configuring component Instances – Configuration Specification – Generate Statements – generating iterative structure – Conditionally generating structures – Configuration of generate Statements.
Case Study: The DLX Computer System.

UNIT V ADTs AND FILES 9

Access Types – Linked Data structures – Abstract Data Types using Packages – Files and Input/Output – Files – The Package Textio – Verilog.
Case Study: Queuing Networks.

Total: 45

TEXT BOOK

1. Peter J.Ashenden, The Designer's Guide to VHDL, Morgan Kaufmann Publishers, San Francisco, Second Edition, May 2001.

REFERENCES

1. Zainalabedin Navabi, VHDL Analysis and Modeling of Digital Systems, McGraw Hill International Editions, Second Edition, 1998.
2. James M.Lee, Verilog Quick start, Kluwer Academic Publishers, Second Edition, 1999.

ES5009 – DATA COMMUNICATION AND NETWORKS

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UNIT I INTRODUCTION 9

Components of network – Topologies – WAN / LAN – OSI – ISO layered Architecture Modulation and demodulation – Bit error rates – Line coding – Error correcting codes.

UNIT II DATA LINK LAYER 9

Design issues – CRC technique and sliding window techniques – Performance analysis of sliding window techniques – Framing formats – Case Study – HDLC protocols – Medium access control – CSMA / CD – Token ring and token bus – FDDI – Wireless LAN – Performance analysis of MAC protocols – Bridges.

UNIT III NETWORK LAYER 9

Circuit switching – packet switching – Design issues – IP addressing and IP diagram – Routers and gateways – Routing –Sub netting – CIDR – ICMP – ARP – RARP – Ipv6 – QoS.

UNIT IV TRANSPORT LAYER 9

TCP and UDP – Error handling and flow control – Congestion control – TCP Retransmission – Timeout – Socket Abstraction.

UNIT V APPLICATION SERVICES 9

Simple Mail Transfer Protocol (SMTP) – File Transfer Protocols (FTP) – telnet - the World Wide Web (WWW) - Hypertext Transfer Protocol (HTTP) - Domain name service (DNS) - Security - Multimedia applications.

Total: 45

REFERENCES

1. William Stallings, “Data and Computer Communications”, Seventh Edition, Prentice Hall, 2003.
2. Larry Peterson, Bruce S Davie “Computer Networks: A Systems Approach”, Morgan Kaufmann Publishers, 2nd Edition, 1999.
3. James F Kurose, “Computer Networking: A Top – Down Approach Featuring the Internet”, Addison Wesley, 2nd Edition 2002.
4. W.Richard Stevens and Gary R Wright, “TCP / IP Illustrated”, Addison Wesley, Volume 1 & 2, 2001.
5. Douglas E Corner, “Internetworking with TCP / IP”, Volume 1 & 2, 2000.

ES5010 – MULTIMEDIA SYSTEMS

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UNIT I MULTIMEDIA 9

Introduction – Multimedia modalities, Channels and Medium – Interaction – Communicative Interaction – Objects and Agents – Channels of Communication – Artificial Languages – Natural Communication – Meta-languages – Components of Interactive Multimedia Systems.

UNIT II KNOWLEDGE AND USER UNDERSTANDING 9

Knowledge – Basic idea of knowledge – A working definition – Knowledge representation – Knowledge Elicitation – Know about user applying user knowledge – acquiring user knowledge – User profiling – User modelling.

UNIT III INTERACTION, INTERFACE & SEMIOTICS 9

Traditional HCI – Modalities and the interface – Interface channels – Functionality and usability – Visual appearance and Graphic design – Multimedia content – Semiotics – Idea of a Sign – Comples Signs – Semiotics and Media.

UNIT IV TEXT AND SOUND 9

Visual Perception of Text – Images on Page – Meaning and Text Readability – Text and the Screen – Modality of Sound – Channels of Communication – Combining Sound Chanles – Technology of Sound – MIDI.

UNIT V IMAGES 9

Psychology of vision – Representational Images – Juxtaposition of Images – Perception of Motion – Constructing a Shot – Shots into narrative – Modern languages of film and television.

Total: 45

REFERENCE

1. Mark Elsom-Cook, “Principles of Interactive Multimedia” McGraw Hill, International Edition 2001.

AN5005 – ASIC DESIGN

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UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS 9

Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 Altera FLEX – Design systems – Logic Synthesis – Half Gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation**.**

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis – VHDL and logic synthesis - Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition – FPGA partitioning – partitioning methods – floor planning – placement – physical design flow – global routing – detailed routing – special routing – circuit extraction – DRC**.**

Total: 45

TEXT BOOK

1. M.J.S. SMITH, “Application – Specific Integrated Circuits” – Addison – Wesley Longman Inc., 1997.

REFERENCES

1. Andrew Brown, “VLSI Circuits and Systems in Silicon”, McGraw Hill, 1991.
2. S.D.Brown, R.J.Francis, J.Rox, Z.G.Uranesic, “Field Programmable Gate Arrays” – Kluever Academic Publishers, 1992.
3. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing”,McGraw Hill, 1994.
4. S.Y. Kung, H.J.Whilo House, T.Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
5. Jose E.France, Yannis Tsividis, “Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing”, Prentice Hall, 1994.

ES5011 – ADVANCED MICROPROCESSORS AND MICRO CONTROLLERS DESIGN

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UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction set – Data formats – Instruction formats – Addressing modes – Memory Hierarchy – register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC – RISC properties – RISC evaluation – On-chip register files versus cache evaluation.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

The software model – functional description – CPU pin descriptions – RISC concepts – bus operations – Super scalar architecture – pipe lining – Branch prediction – The instruction and caches – Floating point unit – protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts – Input/Output – Virtual 8086 model – Interrupt processing – Instruction types – Addressing modes – Processor flags – Instruction set – Basic programming the Pentium Processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE: ARM 9

The ARM architecture – ARM organization and implementation – The ARM instruction set – The thumb instruction set – Basic ARM Assembly language program – ARM CPU cores.

UNIT IV MOTOROLA 68HC11 MICRO CONTROLLERS 9

Instructions and addressing modes – operating modes – Hardware reset – Interrupt system – Parallel I/O ports – Flats – Real time clock – Programmable timer – pulse accumulator – serial communication interface – A/D converter – hardware expansion – Basic Assembly Language programming.

UNIT V PIC MICRO CONTROLLER 9

CPU Architecture – Instruction set – Interrupts – Timers – Memory – I/O port expansion – I^2C bus for peripheral chip access – A/D converter – UART.

Total: 45

REFERENCES

1. Daniel Tabak, “Advanced Microprocessors” McGraw Hill. Inc., 1995.
2. James L. Antonakos , “The Pentium Microprocessor” Pearson Education, 1997.
3. Steave Furber, “ARM system – on – chip architecture” Addison Wesley, 2000.
4. Gene. H.Miller, “Micro Computer Engineering”, Pearson Education, 2003.
5. John.B. Peatman, “Design with PIC Micro controller”, Pearson Education, 1988.
6. James L Antonakos, “An Introduction to the Intel family of Microprocessors” Pearson Education, 1999.
7. Barry B.Breg, “The Intel Microprocessors Architecture, Programming and Interfacing” PHI, 2002.

ES5012 – EMBEDDED COMMUNICATION SOFTWARE DESIGN

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UNIT I **9**

OSI Reference Model – Communication Devices – Communication Echo System – Design Consideration – Host Based Communication – Embedded Communication System – OS Vs RTOS.

UNIT II **9**

Software Partitioning – Limitation of strict Layering – Tasks & Modules – Modules and Task Decomposition – Layer2 Switch – Layer3 Switch / Routers – Protocol Implementation – Management Types – Debugging Protocols.

UNIT III **9**

Tables & other Data Structures – Partitioning of Structures and Tables – Implementation – Speeding Up access – Table Resizing – Table access routines – Buffer and Timer Management – Third Party Protocol Libraries.

UNIT IV **9**

Management Software – Device Management – Management Schemes – Router Management – Management of Sub System Architecture – Device to manage configuration – System Start up and configuration.

UNIT V **9**

Multi Board Communication Software Design – Multi Board Architecture – Single control Card and Multiple line Card Architecture – Interface for Multi Board software – Failures and Fault – Tolerance in Multi Board Systems – Hardware independent development – Using a COTS Board – Development Environment – Test Tools.

Total: 45

REFERENCES

1. Sridhar .T, “Designing Embedded Communication Software” CMP Books, 2003.

ES5013 – DSP INTEGRATED CIRCUITS

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UNIT I DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system, Redundant Number system, Residue Number System. Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

Total: 45

REFERENCES

1. Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York.
2. A.V.Oppenheim et.al, 'Discrete-time Signal Processing' Pearson education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second edition, Pearson edition, Asia.
4. Keshab K.Parhi, 'VLSI digital Signal Processing Systems design and Implementation' John Wiley & Sons, 1999.

CI5102 – DIGITAL SIGNAL PROCESSING

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UNIT I DISCRETE TIME SIGNALS AND SYSTEMS 9

Representation of discrete time signal – classifications – Discrete time – system – Basic operations on sequence – linear – Time invariant – causal – stable – solution to difference equation – convolution sum – correlation – Discrete time Fourier series – Discrete time Fourier transform.

UNIT II FOURIER AND STRUCTURE REALIZATION 9

Discrete Fourier transform – properties – Fast Fourier transform – Z-transform – structure realization – Direct form – lattice structure for FIR filter – Lattice structure for IIR Filter.

UNIT III FILTERS 9

FIR Filter – windowing technique – optimum equiripple linear phase FIR filter – IIR filter – Bilinear transformation technique – impulse invariance method – Butterworth filter – Tchebyshev filter.

UNIT IV MULTISTAGE REPRESENTATION 9

Sampling of band pass signal – antialiasing filter – Decimation by a n integer factor – interpolation by an integer factor – sampling rate conversion – implementation of digital filter banks – sub-band coding – Quadrature mirror filter – A/D conversion – Quantization – coding – D/A conversion – Introduction to wavelets.

UNIT V DIGITAL SIGNAL PROCESSORS 9

Fundamentals of fixed point DSP architecture – Fixed point number representation and computation – Fundamentals of floating point DSP architecture – floating point number representation and computation – study of TMS 320 C 54XX processor – Basic programming – addition – subtraction – multiplication – convolution – correlation – study of TMS 320 F2XXX processor – Basic programming – addition – subtraction – multiplication – convolution – correlation.

Total: 45

REFERENCES

1. John G.Proakis, Dimitris G.Manolakis, “Digital Signal Processing: Principles, Algorithms and Applications”, PHI.
2. S.Salivahanan, A.Vallavaraj and C.Gnanapriya “Digital Signal Processing, TMH, 2000.
3. A.V. Oppenheim and R.W.Schafer, Englewood “Digital Signal Processing”, Prentice-Hall, Inc, 1975.
4. Rabiner and Gold, “Theory and Application of Digital Signal Processing, A comprehensive, Industrial – Strength DSP reference book.
5. B.Venkatramani & M.Bhaskar, “Digital Signal Processors architecture, programming and applications”, TMH, 2002.